FINAL REPORT

PROJECT NO. 1031

GRAVITATIONAL EFFECTS ON PROCESS-INDUCED DISLOCATIONS IN SILICON

By W. A. Porter and Donald L. Parker

Prepared for

NASA Marshall Space Flight Center

Contract No. NAS8-29851

September 20, 1974

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I. INTRODUCTION

For the past several years semiconductor manufacturers have been concerned with imperfections that are induced during device fabrication. Considerable effort has been directed toward understanding the causes of these dislocations, and various processing steps have been identified as major contributors to the generation of dislocations. During diffusion thermal gradients sufficient to cause the generation of dislocations are produced. Impurity depositions lead to concentration gradients which also produce stresses that result in dislocation creation. It is further known that the thermal mis-match of the oxide at the oxide-silicon interface can lead to the generation of undesirable imperfections in the wafer. While these steps have been identified as crucial ones in controlling process-induced dislocations, the critical conditions present when the dislocations are generated during each step have not yet been determined. To understand the exact conditions present when dislocations are generated in any one of these steps requires that one be able to separate the various influencing factors. It is necessary then to be able to selectively create the dislocations while maintaining control of all the critical parameters. One critical parameter which has been largely ignored is the gravitational stress in the wafer which is ever present in all earth bound processing experiments.

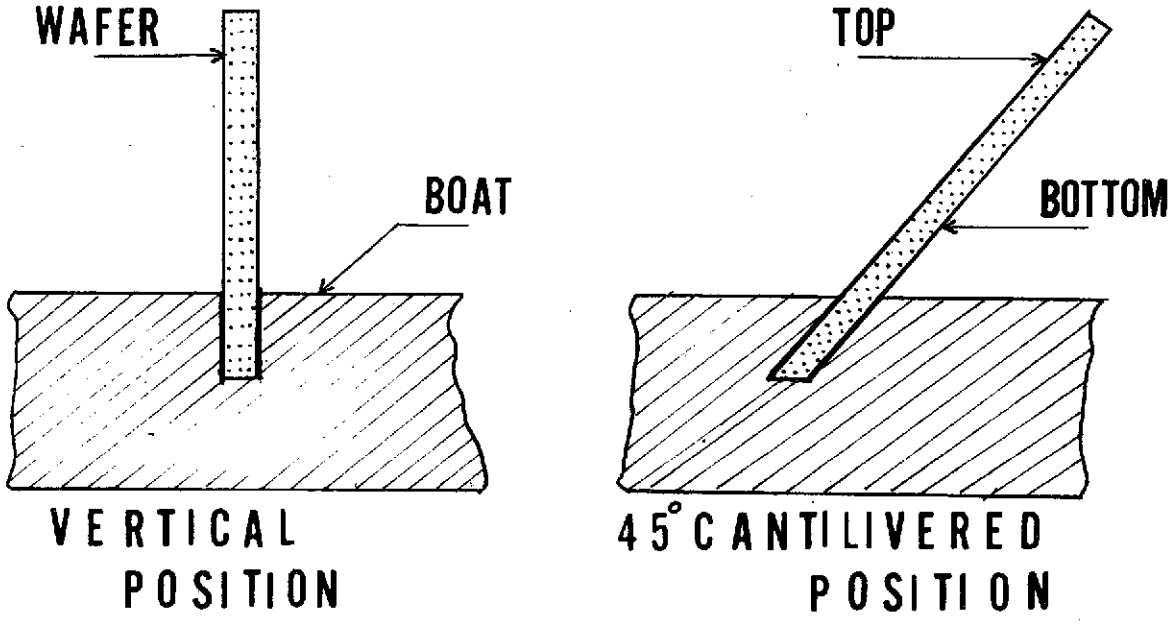
The primary objective of this research has been to establish the role played by gravitational stresses in process-induced defect generation.

II. One-g Processing Experiments

A. Experimental Procedures

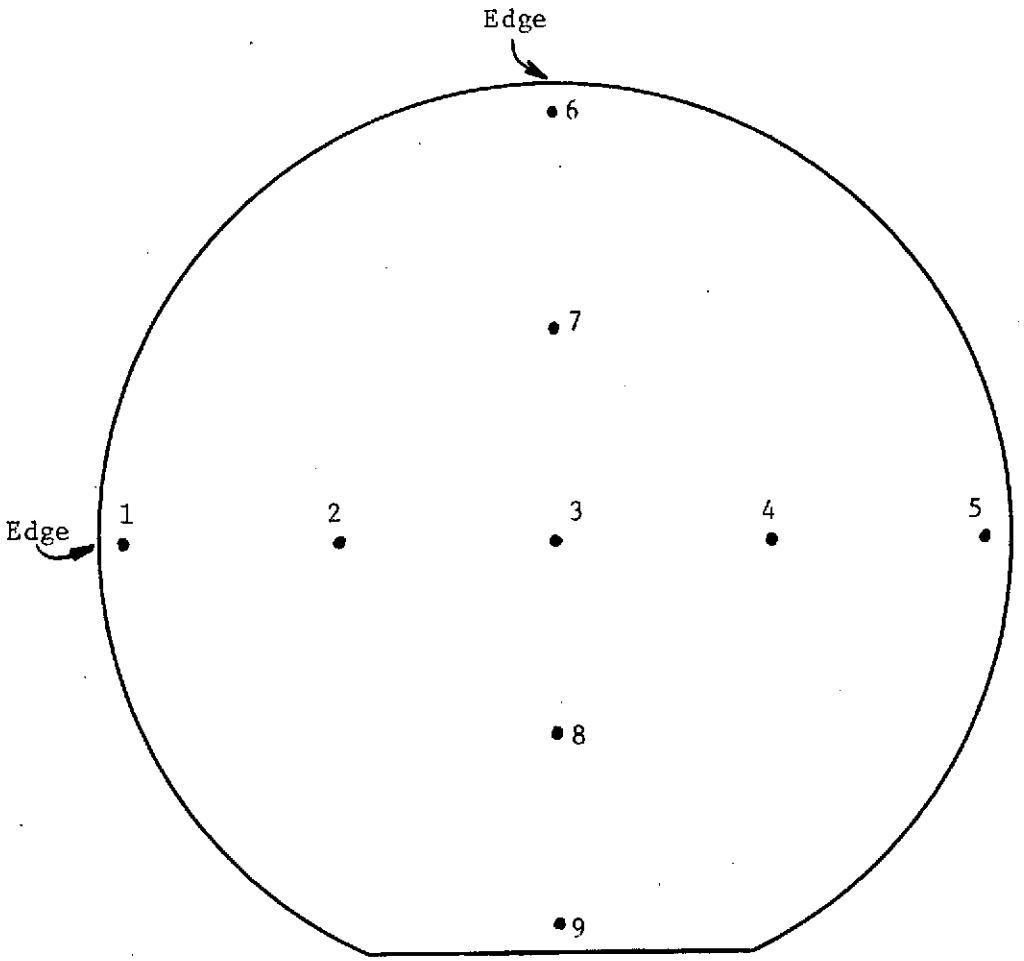
The primary objective of these initial experiments has been to demonstrate the influence of gravity on creating dislocations in silicon wafers during thermal cycling. Thus, thermal cycling of silicon wafers were performed in a controlled ambient where no impurities were present and oxidation was minimum. Both n and p type silicon wafers having a diameter of 1.25 to 1.5 inches with {111} orientation and 8-16 Ω-cm resistivity were used. These wafers were positioned either individually or in pairs on a specially designed quartz carrier which supported the wafers at the bottom edge. The carrier has slots which allows the wafers to be supported either vertically or at a 45° cantilevered position. These positions are shown in Figure 1 which also indicates the "top" and "bottom" surfaces for the inclined wafers.

The surface dislocation densities were measured quantitatively by the well-known Sirtl etch technique. The wafers were immersed in the etch solution from two to five minutes. This etching procedure produced an etch pit at the site of each dislocation intersection with the wafer surface. The etch pits were then counted under microscope inspection at each of the standard ASTM positions. The location of the nine standard ASTM positions is shown in Figure 2 for 1.25" wafers. This technique requires that the wafer surface under examination be highly polished. Several wafers from each batch of starting material that was used were Sirtl etched and all were found to have a negligible background density of dislocations. All the wafers used in this study were thermally cycled under varying conditions described in the following sections and the process-induced dislocations were revealed using the Sirtl etch technique.



WAFER ORIENTATION

Figure 1



Location of Count Position on Wafer

Field 1, 6 : 2.8 mm from edge
Field 2, 7 : 7.3 mm from edge
Field 3 : 16 mm from edge
Field 4, 8 : 24.7 mm from edge
Field 5, 9 : 29.2 mm from edge

Field of View: 0.11 mm^2

Figure 2

B. Results on Vertically Standing Wafers

In order to separate as much as possible the influencing factors referred to in the introduction a large number of wafers were thermally cycled in the vertical position varying: 1) the insertion - withdrawal rate, 2) the furnace flat zone temperature, and 3) the duration of the thermal cycle. Some of these results are shown in Table I for 1250°C and Table II for 1050°C. These results indicate that an insertion - withdrawal rate of up to 2 in/min is sufficiently slow to minimize defect generation due to thermal gradient stresses with the particular low thermal mass carriers that were used in all these experiments. The determination of this maximum insertion - withdrawal rate was one of the primary objectives of this series of thermal cycles. However the most significant features of the results shown in these Tables is the increasing damage done as the cycle duration is increased. Also the amount of damage done for a given cycle duration increases rapidly with increasing temperature. For example, about the same amount of damage is done in 12 to 15 minutes at 1250°C as in one to three hours at 1050°C

C. Results on Wafers Cycled in the 45° Cantilevered Position

Using the 2 in/min insertion-withdrawal rate established during the vertical cycling experiments, wafers were cycled in the 45° cantilevered position in the following ways: 1) Two wafers, one with the polished side up and one with the polished side down 2) Wafers with both sides polished. It is important to note in this case that the gravitational stress produced a compressional deformation on the wafer's bottom side and a stretching deformation on its top side. These experiments were run with furnace temperatures ranging between 1000°C and 1250°C. After thermal cycling, each wafer was given a 2 minute etch to remove the (very thin) oxide. Then,

Table I

WAFERS CYCLED VERTICALLY AT 1250° C

Sample	Temp. C	Stay (Time)	Push in (Withdraw) rate	Loc.#1 Etch Pits	Loc.#2 Etch Pits	Loc.#3 Etch Pits	Loc.#4 Etch Pits	Loc.#5 Etch Pits	Loc.#6 Etch Pits	Loc.#7 Etch Pits	Loc.#8 Etch Pits	Loc.#9 Etch Pits
#39	1250	15 sec	very fast	10^2	2	0	4	96	2	0	0	10^3
#40	1250	0	4in/min	3	10	2	0	75	0	2	6	78
#41	1250	0	2in/min	10	9	0	0	83	0	2	12	97
#42	1250	0	1in/min	14	8	0	9	25	7	2	0	107
#43	1250	15 sec	1in/min	27	12	37	21	39	29	39	41	143
#44	1250	15 sec	24in/min	0	0	0	0	0	1	0	1	22
#45	1250	1 min	24in/min	0	2	0	0	13	1	0	42	54
#46	1250	3 min	24in/min	10	24	0	15	10	2	0	0	37
#47	1250	6 min	24in/min	102	2	3	3	116	5	0	86	142
#48	1250	12 min	24in/min	6	7	20	68	6	63	7	52	78
#49	1250	12 min	24in/min	23	6	1	7	33	15	5	41	$4x10^2$
#50	1250	15 min	24in/min	107	$6x10^2$	$4x10^2$	$6x10^2$	$2x10^2$	$4x10^2$	98	$3x10^2$	$5x10^2$
#51	1250	15 min	24in/min	10^3	10^3	$5x10^2$	$6x10^2$	10^3	63	92	10^3	10^3
#52	1250	20 min	24in/min	$2x10^2$	$5x10^2$	$2x10^2$	$2x10^2$	$4x10^2$	$3x10^3$	$3x10^3$	10^2	10^3
#54	1250	12 min	24in/min	32	5	60	73	92	7	21	$5x10^2$	10^3
#55	1250	13 min	24in/min	21	$2x10^2$	44	$3x10^3$	10^3	$5x10^2$	6x102	10^3	$5x10^3$
#56	1250	14 min	24in/min	23	62	52	$4x10^3$	$3x10^3$	7	15	10^3	10^3
#57	1250	15 min	24in/min	13	$3x10^2$	112	$4x10^3$	53	22	6	10^3	10^3

Notes:

(1) The numbers on this table are the etch pits counted within the field of view ($0.11mm^2$).

(2) All wafers were Sirtl etched for 4 minutes.

(3) All wafers were vertically placed on low mass quartz boat while baking.

Table II

WAFERS CYCLED VERTICALLY AT 1050° C

Sample Number	Temp.	Time Stay	Rush Rate	Loc.#1 Pits	Loc.#2 Pits	Loc.#3 Pits	Loc.#4 Pits	Loc.#5 Pits	Loc.#6 Pits	Loc.#7 Pits	Loc.#8 Pits	Loc.#9 Pits
#58	1050	30min	1min	3	12	6	11	39	7	7	20	23
#59	1050	1hr	1min	34	45	38	29	46	88	69	10^2	$3x10^2$
#60	1050	1hr 30min	1min	20	6	1	7	39	25	7	49	$4x10^2$
#61	1050	2hr	1min	10^2	60	$5x10^2$	79	$4x10^2$	10^2	10^2	46	10^3
#62	1050	1hr 30min	1min	35	77	10^2	67	94	45	7	10^2	10^3
#63	1050	2hr	1min	10^2	10^2	57	9	$6x10^2$	102	31	10^2	10^2
#64	1050	3hr	1min	10^3	10^3	$5x10^2$	60	10^2	10^3	66	10^3	$3x10^3$
#65	1050	4hr	1min	10^2	10^3	10^2	10^2	10^3	10^3	57	10^3	10^3

View at each point is a circle, 0.375mm in diameter, or $0.11mm^2$ Silicon wafer, boron doped [111] orientation, flat at (110). All wafers Sirtl etched before baking.

a sequence of Sirtl etches were performed with a total Sirtl etch time of 5 minutes. The dislocation density on the polished side was determined using the standard ASTM 9 position measurement technique under a 175X light microscope. Table III gives average dislocation densities for the five ASTM points nearest the center of the wafer for three typical runs: One wafer polished and inspected on both sides (#82) and two wafers (#83 & #84) cycled simultaneously one with polished side up and one with the polished side down.

The quantitative dislocation density fluctuates from run to run but, the wafer with the polished side down always has more dislocations than the one with the polished side up. The difference in densities from run to run has not yet been explained, but the strong correlation between top and bottom dislocation densities for a given run is preliminary evidence that gravity influences the creation of lattice defects.

Table III

AVERAGE DISLOCATION DENSITY NEAR THE CENTER OF THE WAFERS

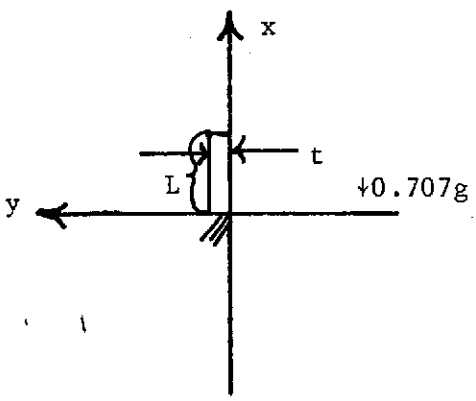
Sample Number	Temperature	Time	Polished Side	Dislocation Count	Average Dislocation Density (per cm^2)
82	1100°C	3 hr	Both	Top	1860
82	1100°C	3 hr	Both	Bottom	4410
83	1150°C	3 hr	Up	Top	435
84	1150°C	3 hr	Down	Bottom	1050

III. Theoretical Analysis of the Gravitational Stresses

Several attempts were made to find a satisfactory means of determining the distribution of stress in the wafers supported in the 45° cantilevered position under the gravitational bending moments. A computer program was tried which uses the finite element method. The results of this technique were found to be very inaccurate when a sufficiently small number (200 for a two-dimensional analysis) of nodal points were chosen to keep the computing costs at a reasonable level. For this reason a closed form calculation was done on a simplified model as follows:

Assume the wafer is a rectangular plate of length, L; thickness, t: and width, w: Since the deformation of the wafer is so small the mass (load) distribution of the wafer is assumed not to change under gravity and that simultaneous stresses may be superimposed. Thus, the stress distribution will be found for a vertically standing wafer in a 0.707g field and then for the wafer supported in a horizontal cantilevered position in a 0.707g field and the resulting stress distributions will be added to obtain the distribution for the wafer supported in the 45° cantilevered position.

V E R T I C A L W A F E R



let ρ = mass density of silicon

λ = weight/unit length

then $\lambda = \frac{.707\ \rho\ g\ L\ w\ t}{L} = \frac{\rho\ g\ w\ t}{\sqrt{2}}$

then σ_{xv} = x-component of stress for vertical case

then $\sigma_{xv} = \frac{\lambda(L-x)}{wt} = \frac{\rho g}{\sqrt{2}}(L-x)$

H O R I Z O N T A L W A F E R

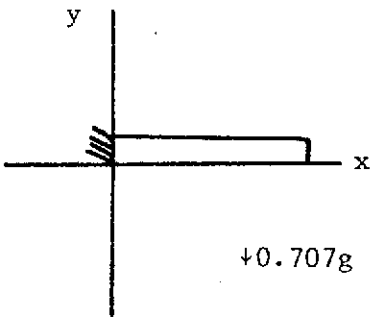
$$\frac{d\phi}{ds} = \frac{M_b}{EI}$$

where $\frac{d\phi}{ds}$ = wafer curvature

M_b = bending movement

E = elastic modulus

$I = \int y^2 dA = 1/12\ w\ t^3$



also $\epsilon_x = \frac{d\phi}{ds}\, y$

where ϵ_x is the strain and y the distance from the central plane

$$\sigma_x = E\epsilon_x = \frac{-d\phi}{ds} Ey = \frac{-M_b}{I} y$$

but $M_b = \lambda(L-x)\left(\frac{L-x}{2}\right)$

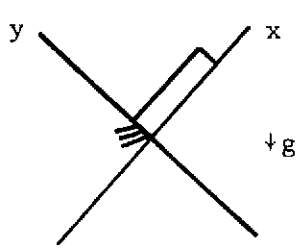
where again $\lambda = \frac{\rho g w t}{\sqrt{2}}$

$$\text{thus } \sigma_{xh} = -\frac{\rho g w t}{2\sqrt{2}\, I} (L - x)^2\, y$$

$$\sigma_{xh} = -\frac{6\rho g}{\sqrt{2}\, t^2} (L - x)^2\, y$$

4 5 ° C A N T I L E V E R P O S I T I O N

$$\sigma_x = \sigma_{xv} + \sigma_{xh}$$



$$= \frac{\rho g}{\sqrt{2}} \left\{(L-x) - \frac{6y}{t^2} (L-x)^2\right\}$$

$$= \frac{\rho g L}{\sqrt{2}} \left\{(1-x/L) - \frac{6Ly}{t^2} \left(1-\frac{x}{L}\right)^2\right\}$$

for the surfaces of the wafer $y = \pm t/2$

$$\text{thus } \sigma_x\left(\begin{matrix}\text{top}\\ \text{bottom}\end{matrix}\right) = \frac{\rho g L}{\sqrt{2}} \left\{\left(1 - \frac{x}{L}\right) \pm \frac{3L}{t} (1 - x/L)^2\right\}$$

Notice that the magnitude of the stress at the wafer surface is controlled primarily by the ratio L/t.

for silicon $\rho g = 0.867$ lb/in^3

and taking L = 1.5 inch and t = 0.015 inch we get $\sigma_x\left(\begin{matrix}\text{top}\\ \text{bottom}\end{matrix}\right) = 0.092\{(1 - \frac{x}{L})$

$\pm$ 300 $(1 - x/L)^2\}$ in pounds/in^2

The results are plotted in Figure II.

The conclusions to be drawn from this analysis are summarized as follows:

1. The magnitude of the stresses at the wafer top and bottom surfaces are essentially equal, due mostly to the bending moment, and have opposite sign (compression for the bottom surface and tension for the top surface)

2. The stress is sensitive to the L/t ratio and can be very large for thin wafers.

3. The stress of the surface varies slightly less than one order of magnitude over the ASTM standard points used in the dislocation count correlation.

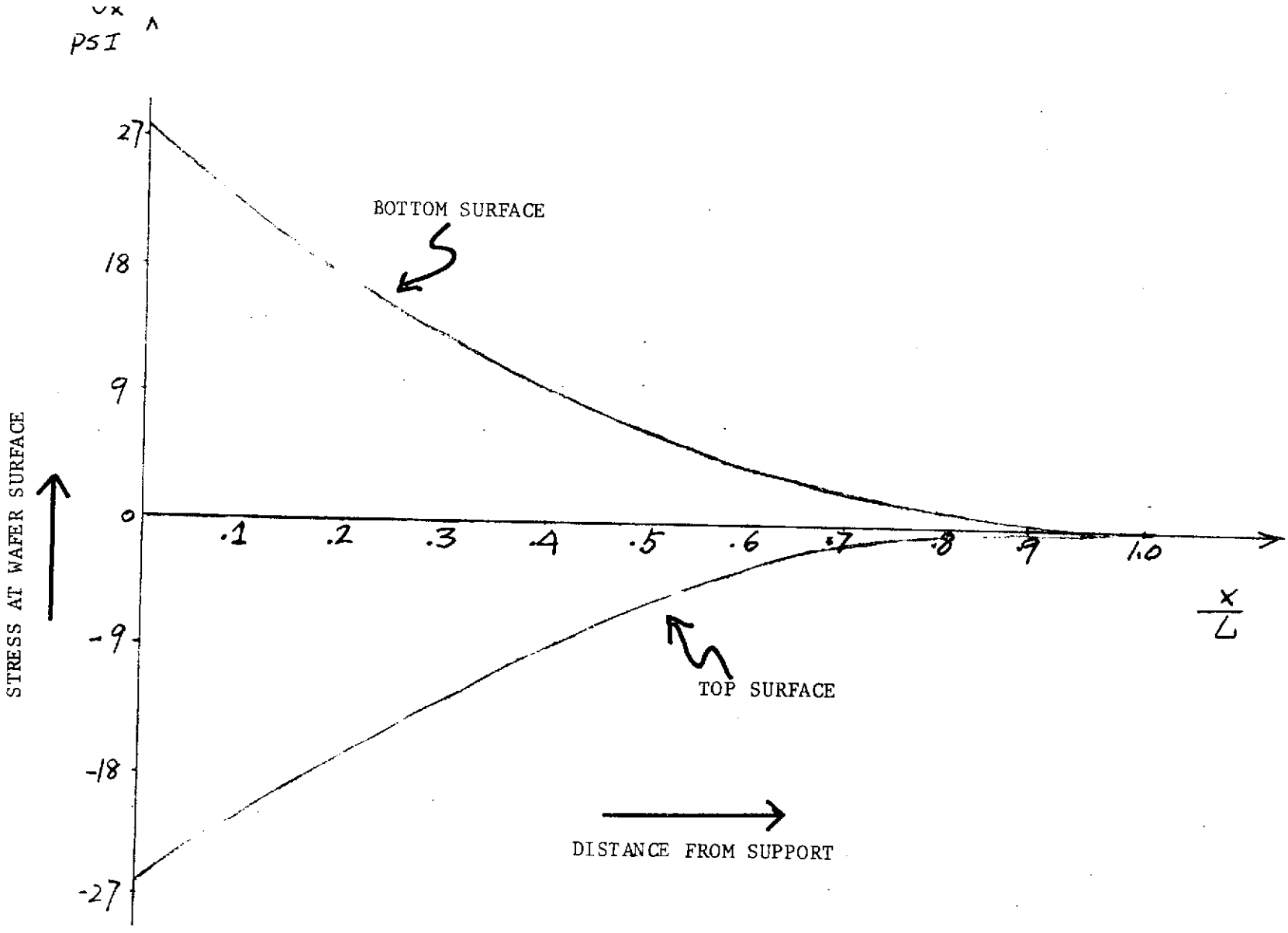

σx
PSI
27
18
9
0
-9
-18
-27
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
BOTTOM SURFACE
TOP SURFACE
STRESS AT WAFER SURFACE
DISTANCE FROM SUPPORT
x/L

Figure II

IV. Correlation of Lattice Defects and Diode Characteristics

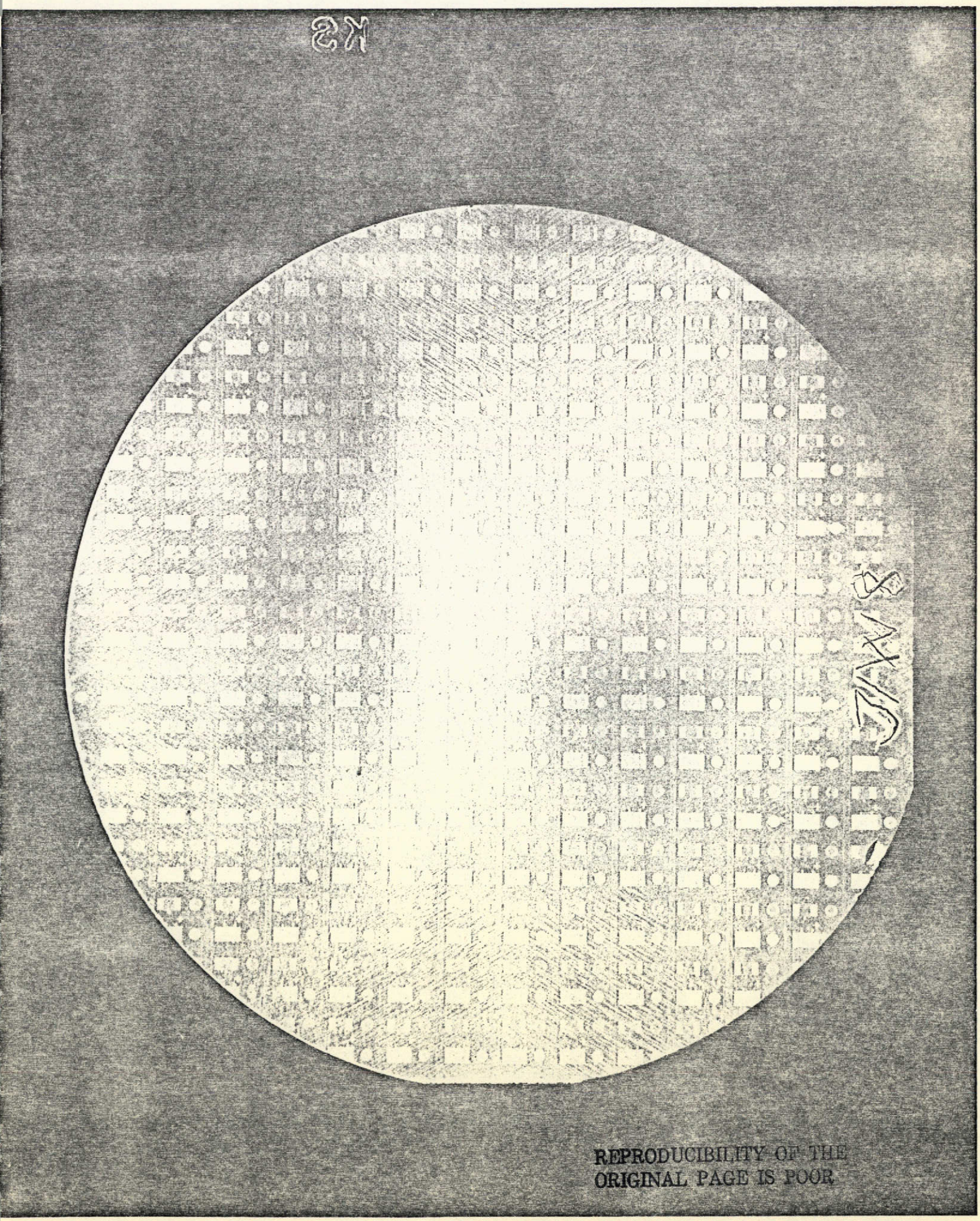
In the course of any study on process-induced defects some attention must be paid to their effects on the finished product. This section correlates, for a particular diode, the reverse bias breakdown voltage and reverse bias leakage current (at 30 volts in darkness) with lattice damage observed by X-ray topography. All the processing steps, measurements, and analysis were done in the laboratories of the Institute for Solid State Electronics.

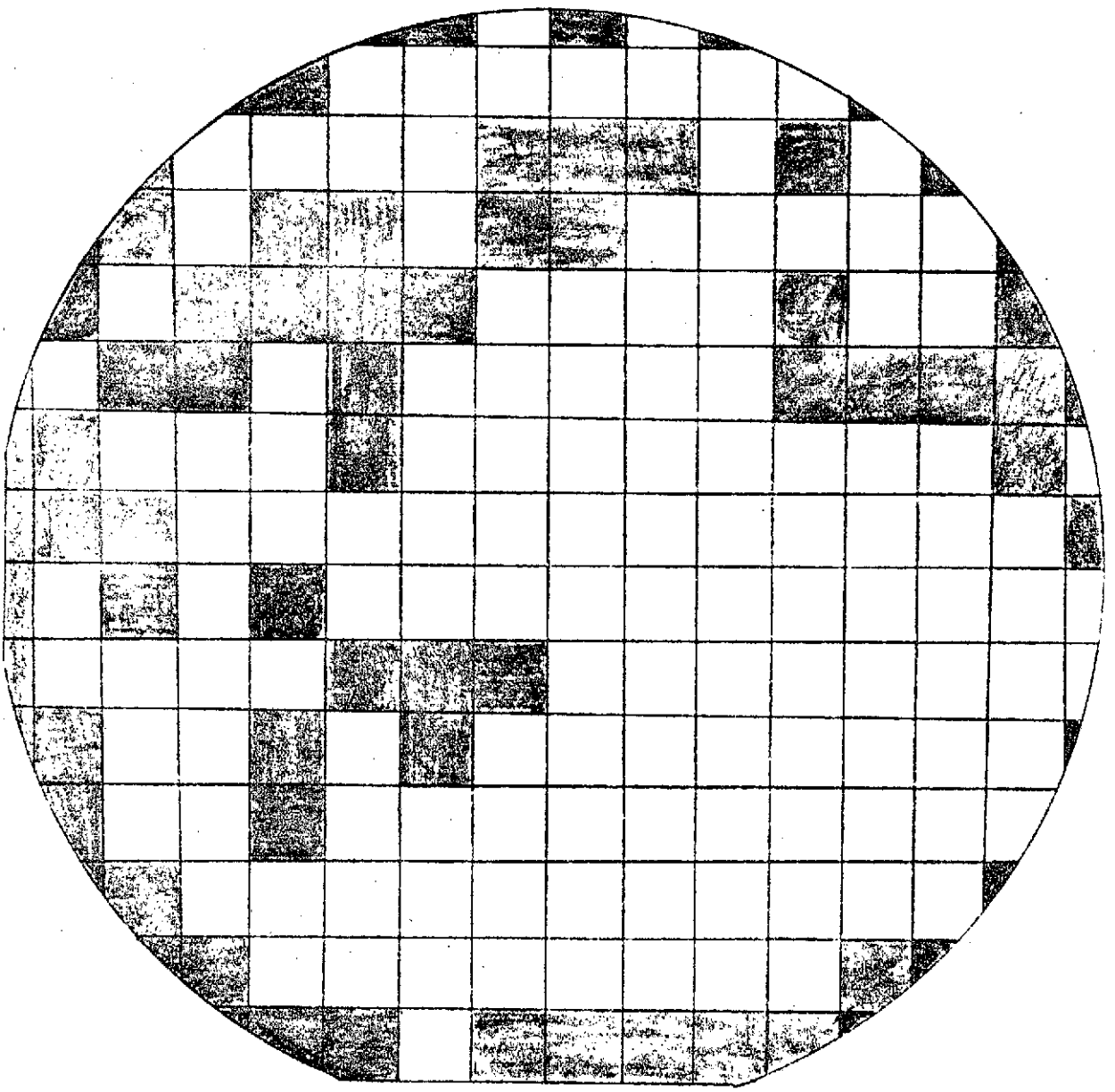
The photograph is a positive enlargement of a Berg-Barrett X-ray topograph of the 1.25" wafer used in this study. A recurring pattern is observed with a cross at the center of each pattern. The diodes can be identified as the round devices located in the lower left corner of each pattern. The bottom of the wafer is taken to be the flat near the "J1W8" notation. The upper left device is a dual gate FET; the upper right device is an FET; and the lower right device is a capacitor. The lattice damage was deliberately produced by very rapid thermal cycling of the wafer in a special boat after diffusion and before metalization. The defects are most easily seen in the xerox copies near the top and sides of the wafer.

The enclosed wafer facsimiles have blackened squares which indicate the diodes that fail to meet a given performance criteria. Most of the "good" diodes have a reverse bias breakdown voltage of 80-85 volts with a few as high as 100 volts. Typical leakage currents for the "good" diodes are in the range 10^{-9} to 10^{-10} amperes.

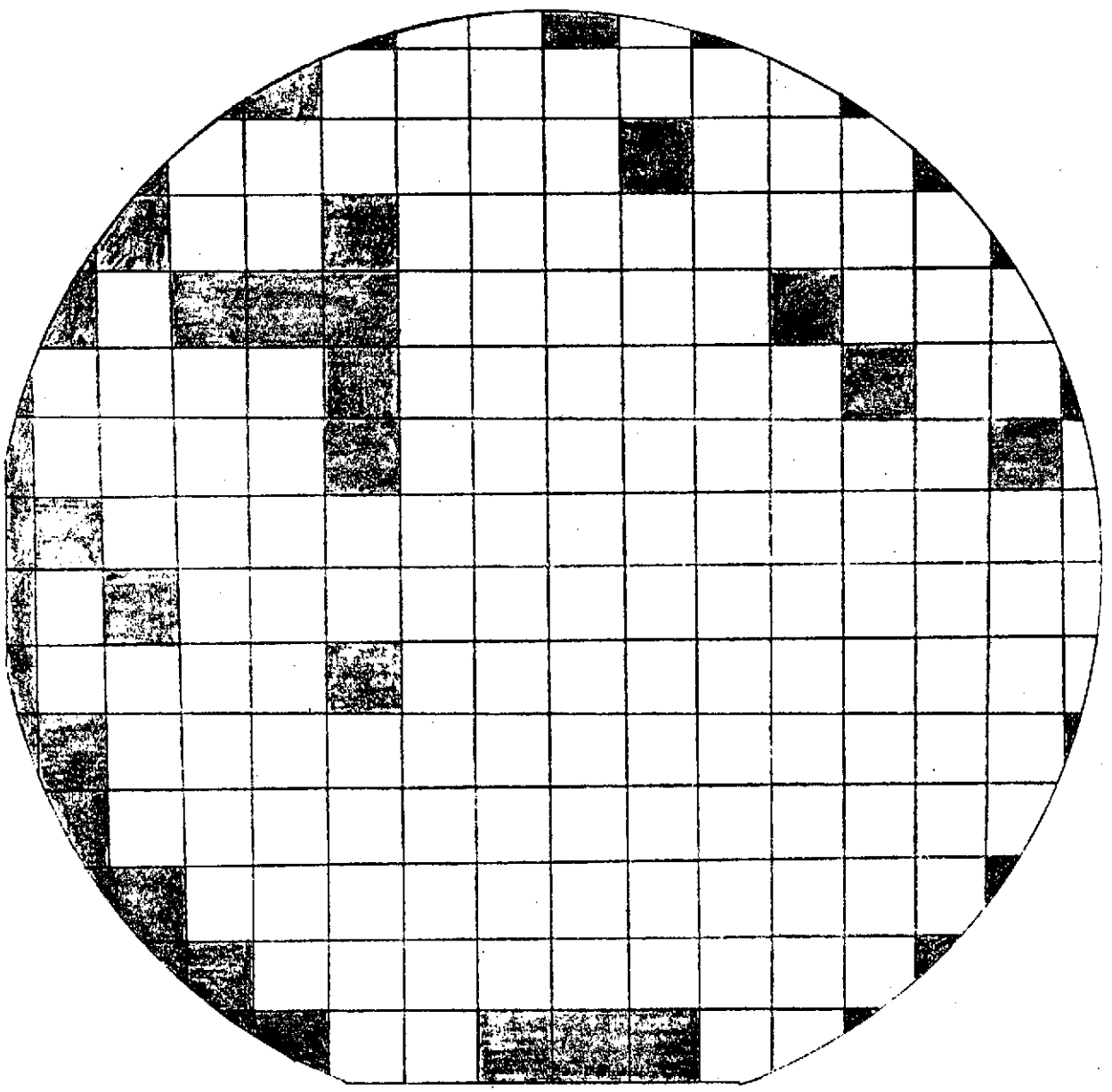
Of the 175 diodes on the wafer, 90 were judged to have some lattice damage within the diode spot by careful examination of the original X-ray negative.

Seventy-nine of the diodes have a reverse bias breakdown voltage of less than 75 volts. Using 75 volts as the pass-fail criteria the existence of lattice defects corresponded to bad devices (or the lack of defects forecast good devices) 124 times out of the 175 cases. While this percentage represents a very good correlation between defect-device influence, had the defects been produced earlier in the process the correlation would probably be even higher.

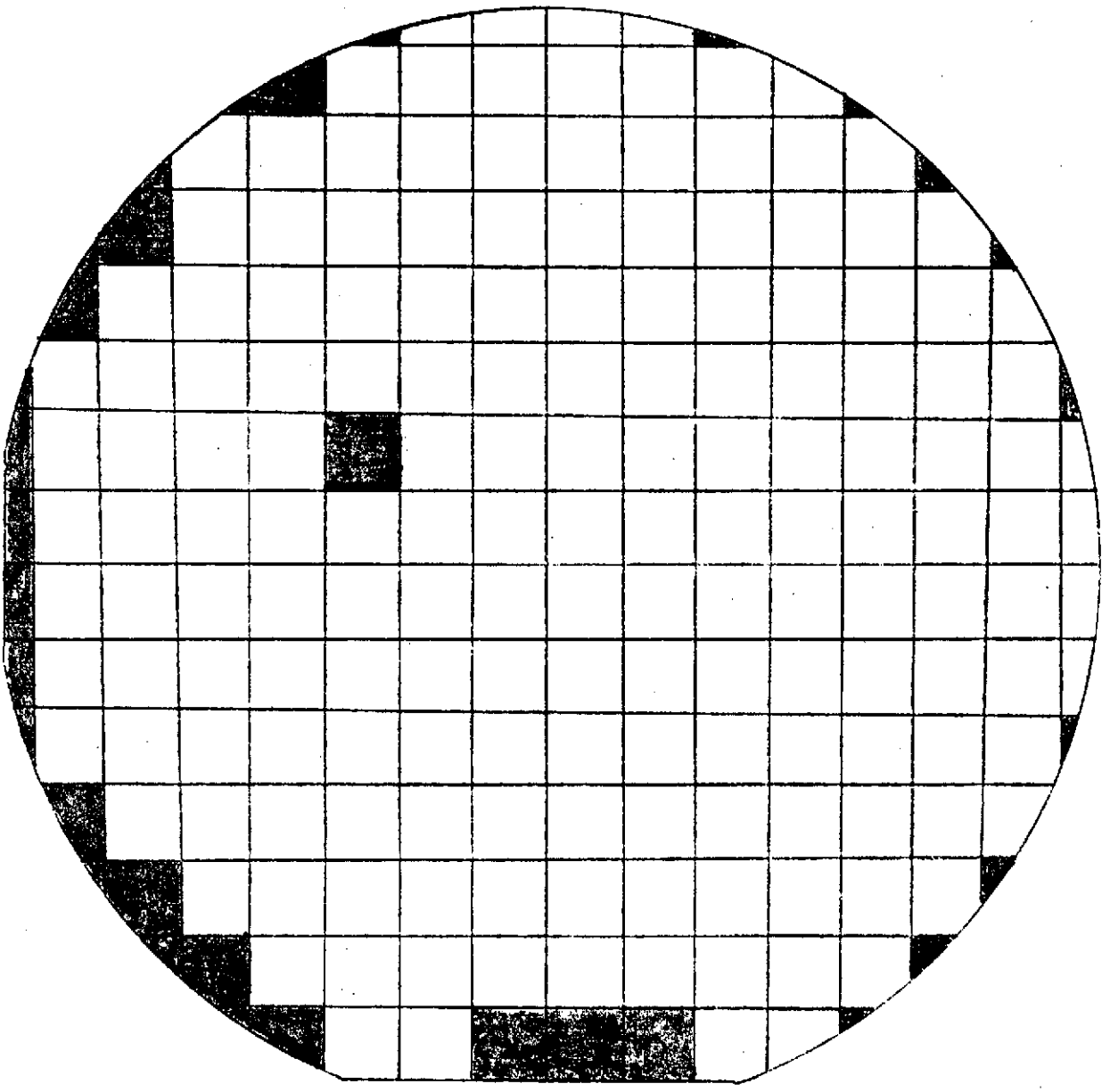




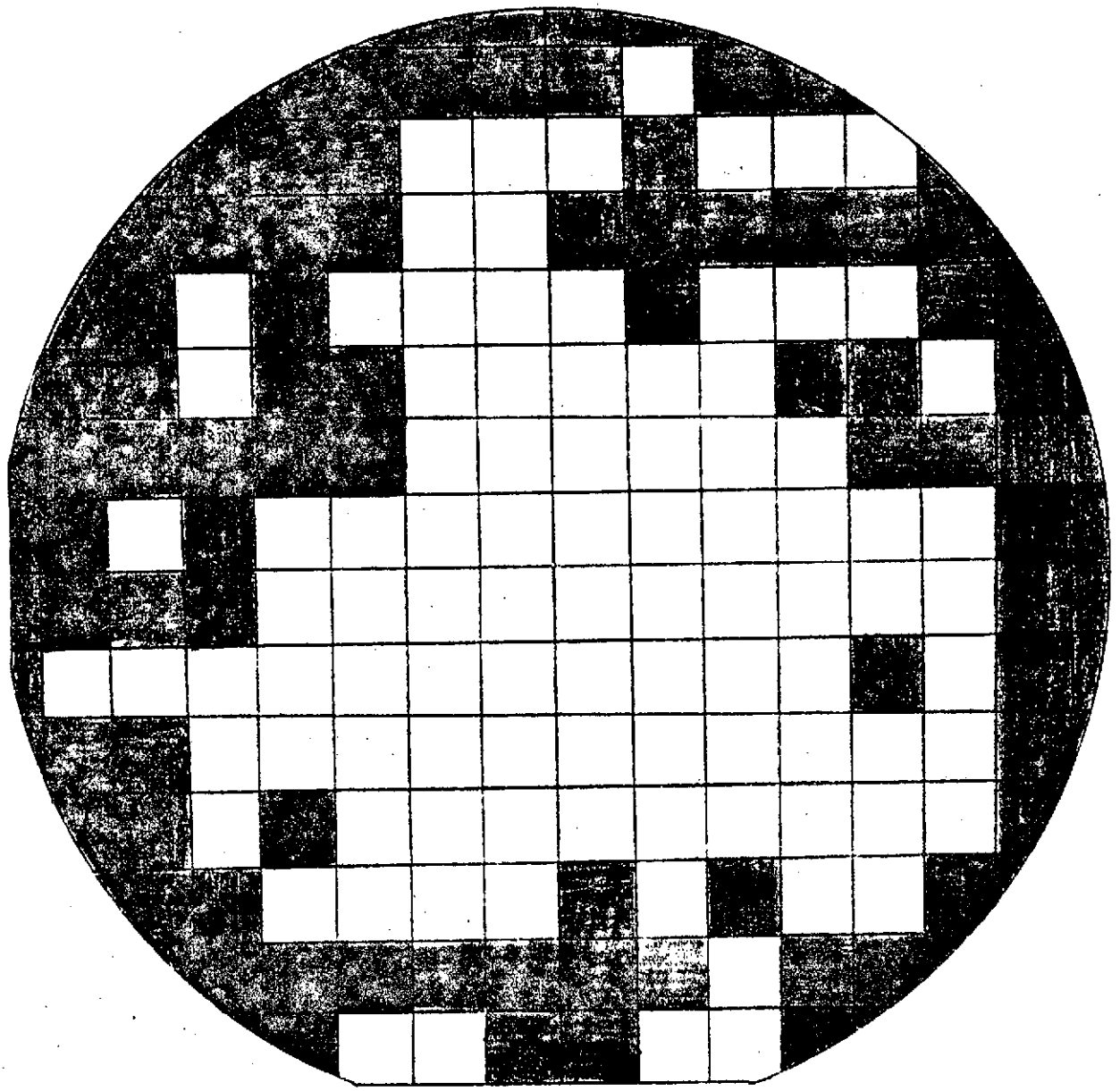
LEAKAGE CURRENT $> 10^{-8}$ AMPS



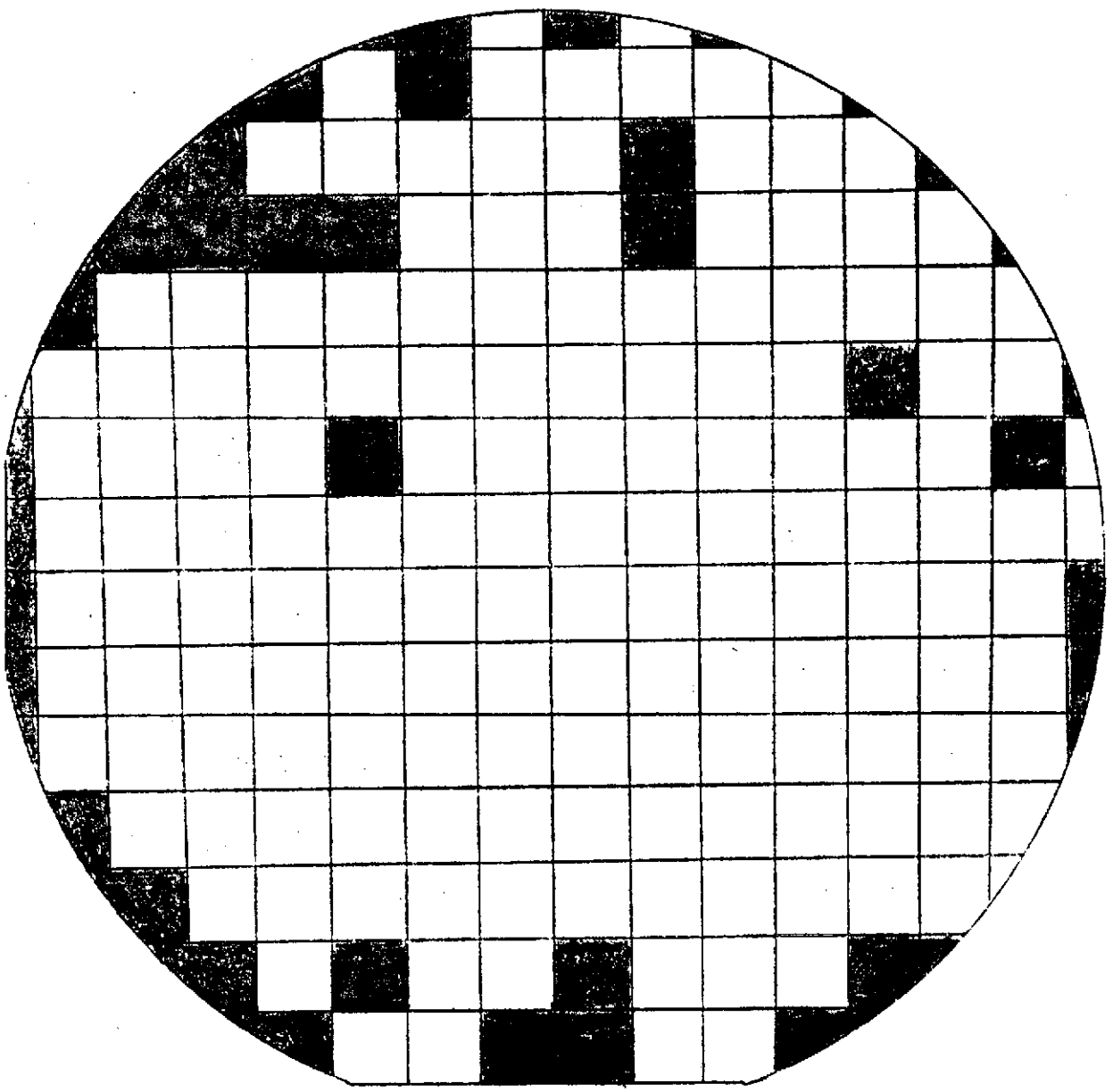
LEAKAGE CURRENT > 10^{-6} AMPS



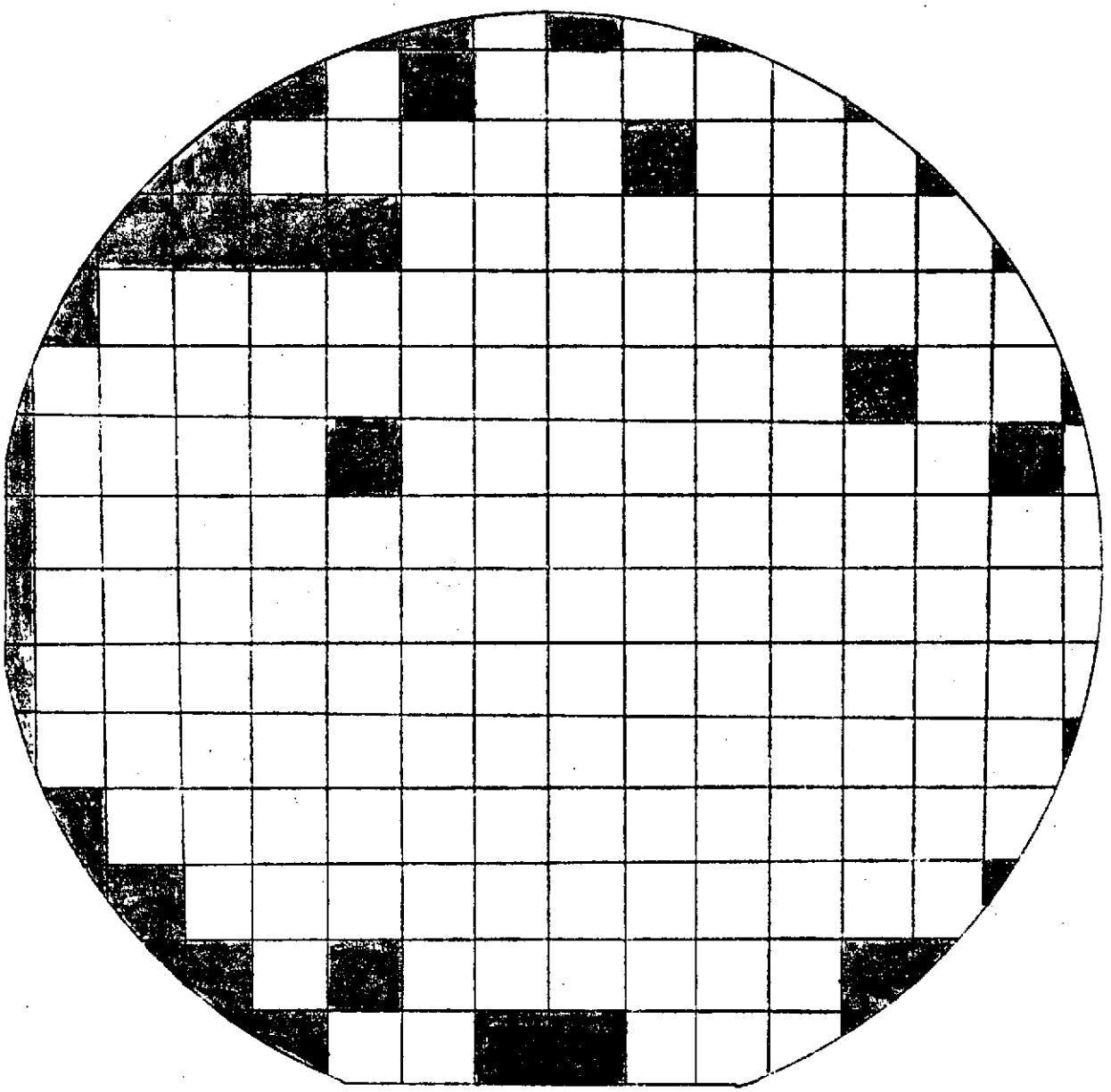
LEAKAGE CURRENT $> 10^{-4}$ AMPS



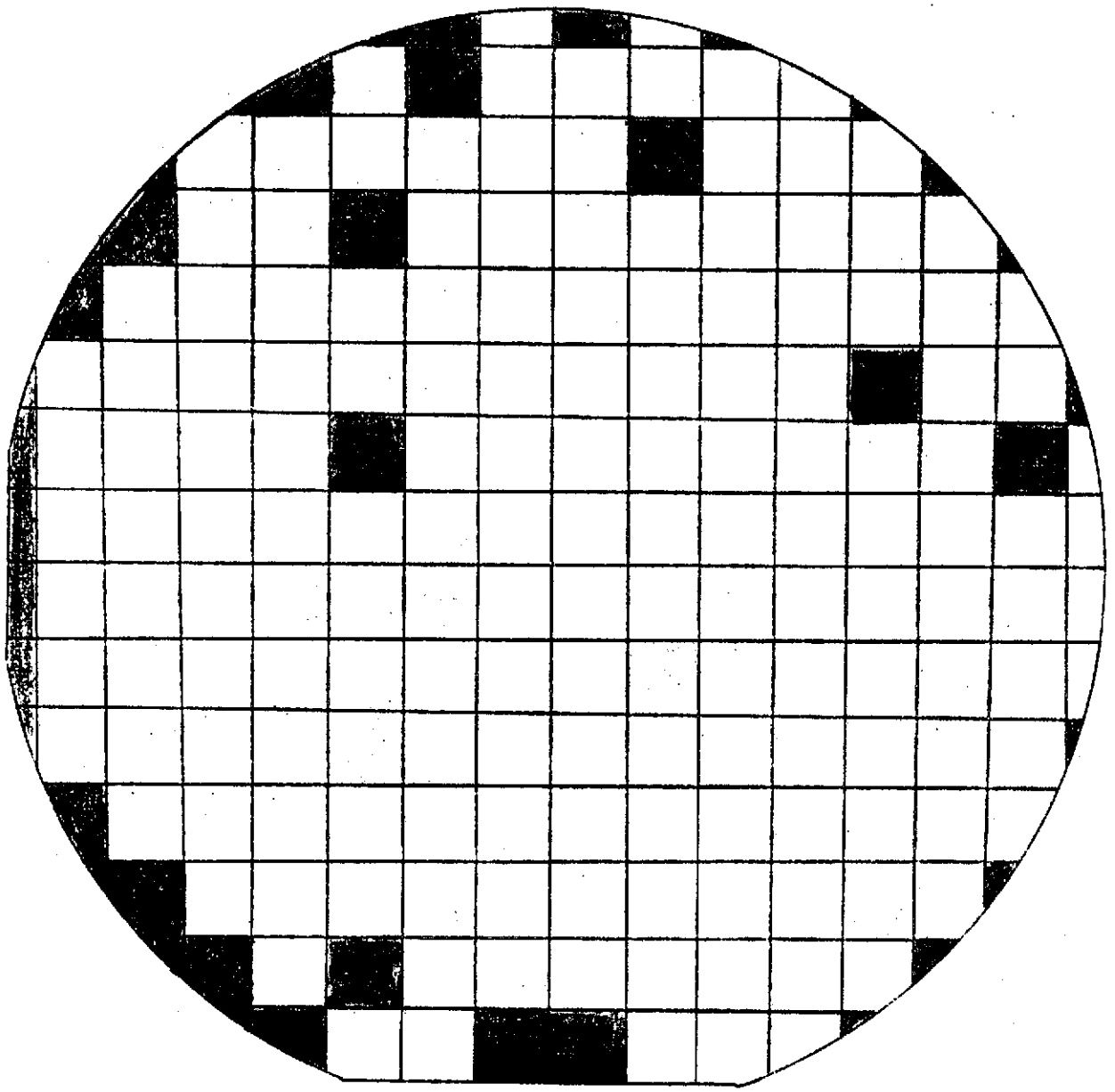
BREAKDOWN VOLTAGE <75 VOLTS



BREAKDOWN VOLTAGE <70 VOLTS



BREAKDOWN VOLTAGE <60 VOLTS



BREAKDOWN VOLTAGE < 50 VOLTS

V. Conclusion and Recommendations

First let us review the purpose of this research as it relates to semiconductor device fabrication. Thermal processing does induce dislocations through a number of well known mechanisms (thermal gradients, oxide interface stresses, impurity gradient stresses, etc.). However, not all the induced defects can be accounted for by these mechanisms and the remainder are generally attributed to "plastic flow". The results on vertically standing wafers conclusively show two significant features of the plastic flow phenomenon:

1. The density of dislocations generated during a given thermal cycle is directly related to the duration of the cycle.
2. The duration of the thermal cycle required to produce a given dislocation density is inversly related to the equilibrium temperature.

While these results by themselves do not prove that gravitationsl stress cause plastic flow, it is certainly a plausible explanation. The experiments on wafers cycled in the 45° cantilevered position were done to produce an asymmetrical top to bottom gravitational stress to establish that gravity does play a role in the production of defects. In examining the results of these 45° experiments recall that there is no acceptable means of predicting which surface (top or bottom) should have the most dislocations under the gravitational bending moments. Thus the fact that there is a contrast in the top - bottom dislocation density in wafers thermally cycled at 45° is further supporting evidence that gravitational stresses contribute to the production of defects. The major point is that the effect may not be subtle at all! The theoretical analysis of the stress distribution shows that the magnitudes of the stress at the top and bottom surfaces are about the same. The experimental results require the conclusion that compressional stress is more likely to produce dislocations. The

most difficult feature of the results to understand is the rather small variation of the defect density across the face of wafers cycled either vertically or at 45°. This could be due to the lack of sufficient data for an accurate statistical analysis but is more likely due to a more complex distribution of gravitational stress than that given by the rather simple mathematical model.

Two general conclusions may be drawn from the efforts put into this research:

1.) Wafers never reach a true thermodynamic equlibrium condition during a thermal cycle.

2.) Gravitational stress does play a role in process-induced defect generation.

The most expedient means for firmly and quantitatively establishing the degree of influence of gravitational stresses in defect generation is to perform identical experiments in other than one-g conditions i.e. centrifuge experiments for greater than one-g and orbital experiments for zero-g. It is possible (or even probable) that defect-free electronic devices could be fabricated in a zero-g environment with virtually 100% yields. In view of the small quanities of material involved, zero-g processing could have significant economic advantages particularly in the fabrication of LSI arrays.